CLAIMS

1. A semiconductor device, comprising:

a semiconductor substrate;

a polysilicon pattern formed on said semiconductor substrate via an insulation film;

an interlayer insulation film formed on said semiconductor substrate so as to cover said polysilicon pattern; and

a metal interconnection layer pattern formed on said interlayer insulation film,

wherein said metal interconnection layer pattern carrying silicon nitride films respectively on a top surface, a bottom surface and sidewall surfaces thereof.

2. The semiconductor device as claimed in claim 1, wherein said silicon nitride films comprises a first nitride film formed on a surface of said interlayer insulation film and in contact with a bottom surface of said metal interconnection layer pattern, and a second nitride film covering said sidewall surfaces and top surface of said metal interconnection layer pattern.

3. The semiconductor device as claimed in claim 2, wherein said first nitride film and said second nitride film have respective, different thicknesses.

4. The semiconductor device as claimed in claim 2, wherein there is provided a region where said first nitride film and said second nitride film are removed except for said first nitride film underlying said metal interconnection layer pattern.

5. The semiconductor device as claimed in claim 1, wherein said semiconductor device further comprises a p-channel MOS transistor having a gate electrode formed of said polysilicon pattern, formation of said metal interconnection layer pattern, said first nitride film and said second nitride film being suppressed in a region over said p-channel MOS transistor.

6. The semiconductor device as claimed in claim 1, wherein there is provided a laminated film between said polysilicon pattern and said interlayer insulation film, said laminated film comprising consecutive lamination of an oxide film and a third

nitride film in a direction from said polysilicon to said interlayer insulation film.

7. The semiconductor device as claimed in claim 6, wherein said semiconductor device further comprises a p-channel MOS transistor having a gate electrode of said polysilicon pattern, said third nitride film being formed over said p-channel MOS transistor.

8. A semiconductor device having a voltage divider circuit producing an output voltage by dividing a voltage supplied thereto,

said voltage divider circuit comprising two or more resistance elements, said output voltage of said voltage divider being adjustable by disconnection of a fuse element,

said resistance element comprising a polysilicon pattern formed on a semiconductor substrate via an insulation film,

an interlayer insulation film being formed on said semiconductor substrate so as to cover said polysilicon pattern,

a metal interconnection layer pattern being formed on said interlayer insulation film,

said metal interconnection layer pattern carrying silicon nitride films respectively on a top surface, a bottom surface and sidewall surfaces thereof.

9. A semiconductor device comprising:

a voltage divider circuit dividing a voltage supplied thereto and producing an output voltage;

a reference voltage generator supplying a reference voltage; and

a comparator circuit comparing said output voltage of said voltage divider circuit with said reference voltage of said reference voltage generator,

said voltage divider circuit comprising two or more resistance elements, said output voltage of said voltage divider being adjustable by disconnection of a fuse element,

said resistance element comprising a polysilicon pattern formed on a semiconductor substrate via an insulation film,

an interlayer insulation film being formed on said semiconductor substrate so as to cover said polysilicon pattern,

a metal interconnection layer pattern being formed on said interlayer insulation film,

said metal interconnection layer pattern carrying silicon nitride films respectively on a top surface, a bottom surface and sidewall surfaces thereof.

10. A semiconductor device, comprising:

an output driver controlling an output of an input voltage;

a voltage divider circuit dividing said output voltage and producing a divided voltage;

a reference voltage generator producing a reference voltage; and

a constant voltage generator having a comparator circuit comparing said divided voltage from said voltage divider circuit and said reference voltage from said reference voltage generator, said comparator circuit controlling said output driver in response to a result of comparison,

said voltage divider circuit comprising two or more resistance elements, said output voltage of said voltage divider being adjustable by disconnection of a fuse element,

said resistance element comprising a

polysilicon pattern formed on a semiconductor substrate via an insulation film,

an interlayer insulation film being formed on said semiconductor substrate so as to cover said polysilicon pattern,

a metal interconnection layer pattern being formed on said interlayer insulation film,

said metal interconnection layer pattern carrying silicon nitride films respectively on a top surface, a bottom surface and sidewall surfaces thereof.

11. A method of fabricating a semiconductor device, comprising the steps of:

forming a polysilicon pattern on a semiconductor substrate via an insulation film;

forming an interlayer insulation film on the semiconductor substrate so as to cover the polysilicon pattern;

forming a first nitride film on the interlayer insulation film;

forming a metal interconnection layer pattern on the first nitride film; and

forming a second nitride film on the first nitride film so as to cover the metal interconnection

layer.

12. The method as claimed in claim 11, further comprising the step, after said step of forming said second nitride film, of removing said second nitride film and said first nitride film selectively from a predetermined area.